NCE N&P-Channel Complementary Power MOSFET

Description

The NCE40NP2815G uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Application

- DC/DC converter
- Power management
- H-Bridge
- Inverter

N-channel

- V_{DS} = 40 V,I_D = 28 A

  $R_{DS(ON)}$< 16.5 mΩ @V_{GS}=10V (typical: 14 mΩ)

  $R_{DS(ON)}$< 22 mΩ @V_{GS}=4.5V (typical: 18 mΩ)

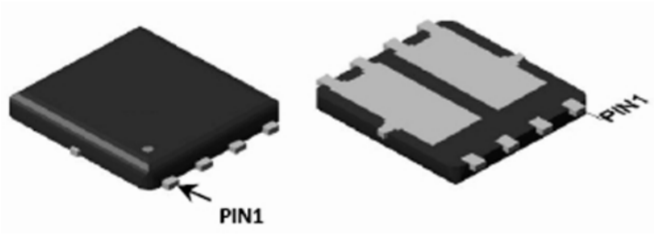
P-channel

- V_{DS} = -40 V,I_D = -15 A

  $R_{DS(ON)}$< 24 mΩ @V_{GS}=-10V (typical: 20.8 mΩ)

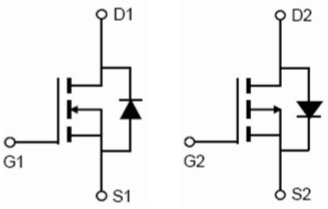
  $R_{DS(ON)}$< 37 mΩ @V_{GS}=-4.5V (typical: 30.3 mΩ)

- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation
- 100% UIS tested
- 100% ΔVds tested



Top View Bottom View

PDFN5×6-8L



N-channel P-channel

Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
40NP2815G	NCE40NP2815G	PDFN5×6-8L	Ø330mm	12mm	5000units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current	I_D	28	-15	A
Continuous Drain Current(T_C=100℃)	I_D(100℃)	23	-15	A
Pulsed Drain Current	I_{DM}	112	-60	A
Maximum Power Dissipation	P_D	35	35	W
Single pulse avalanche energy (Note 1)	E_{AS}	70	64	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150		℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case**(N-channel)**	$R_{\theta JC}$	3.6	℃/W
Thermal Resistance,Junction-to-Case**(P-channel)**	$R_{\theta JC}$	3.6	℃/W
Thermal Resistance,Junction-to-Ambient (Note 2)**(N-channel)**	$R_{\theta JA}$	50	℃/W
Thermal Resistance,Junction-to-Ambient (Note 2)**(P-channel)**	$R_{\theta JA}$	50	℃/W

N-Channel Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=15A	-	14	16.5	mΩ
		V_{GS}=4.5V, I_D=10A	-	18	22	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=11A	-	20	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V F=1.0MHz	-	813	-	pF
Output Capacitance	C_{oss}		-	101	-	pF
Reverse Transfer Capacitance	C_{rss}		-	92	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V ,R_L=2Ω V_{GS}=10V,R_G=3Ω	-	4	-	nS
Turn-on Rise Time	t_r		-	11.5	-	nS
Turn-off Delay Time	$t_{d(off)}$		-	18	-	nS
Turn-off Fall Time	t_f		-	5.6	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=10A, V_{GS}=10V	-	20.8	-	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	nC
Gate-Drain Charge	Q_{gd}		-	5.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=15A	-	-	1.2	V
Diode Forward Current	I_S		-	-	28	A

Notes:

1. EAS condition : Tj=25℃,V_{DD}=35V,V_G=10V,L=0.5mH,Rg=25Ω.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heat sink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

P-Channel Electrical Characteristics (T_C=25℃unless otherwise noted)

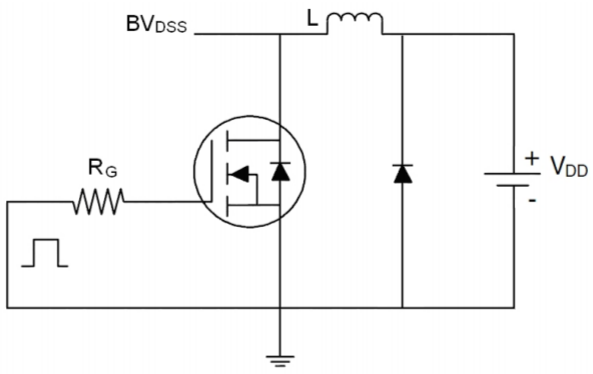
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.0	-1.5	-2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-7A	-	20.8	24	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	30.3	37	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-10A	-	20	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=-20V,V_{GS}=0V F=1.0MHz	-	884	-	pF
Output Capacitance	C_{oss}		-	118	-	pF
Reverse Transfer Capacitance	C_{rss}		-	108	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-20V ,R_L=1.5Ω V_{GS}=-10V,R_G=3Ω	-	11	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	V_{DS}=-20V,I_D=-10A V_{GS}=-10V	-	21.7	-	nC
Gate-Source Charge	Q_{gs}		-	2.8	-	nC
Gate-Drain Charge	Q_{gd}		-	5.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-7A	-	-	-1.2	V
Diode Forward Current	I_S		-	-	-15	A

Notes:

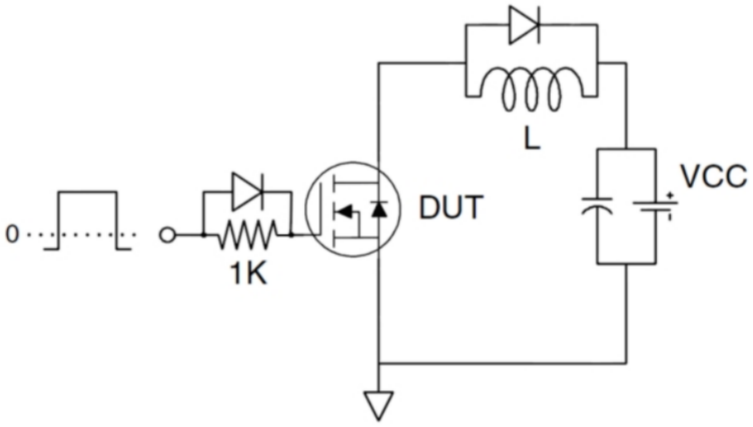
1. EAS condition : Tj=25℃,V_{DD}=-35V,V_G=-10V,L=0.5mH,Rg=25Ω.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heat sink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

Test Circuit

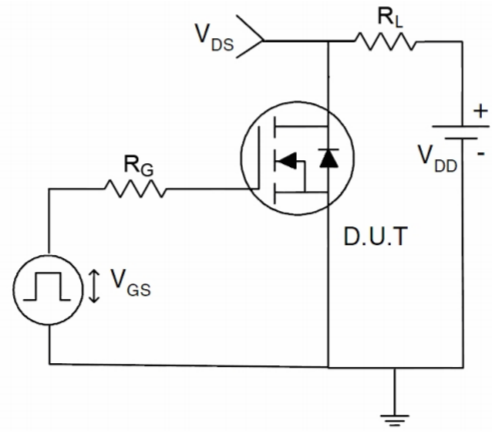
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



N-Channel Typical Electrical and Thermal Characteristics (Curves)

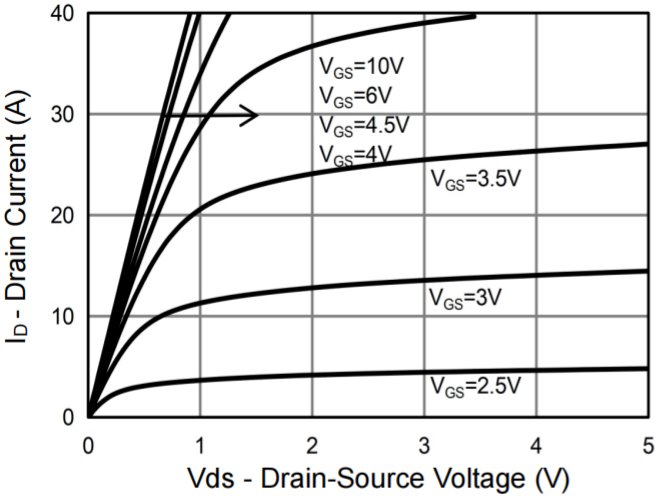


Figure 1 Output Characteristics

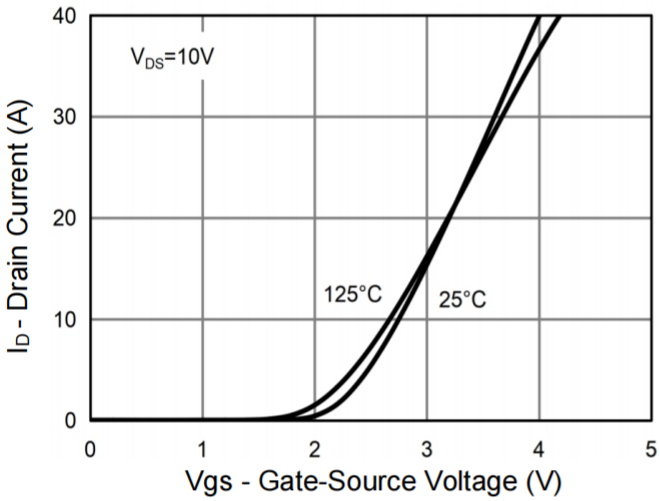


Figure 2 Transfer Characteristics

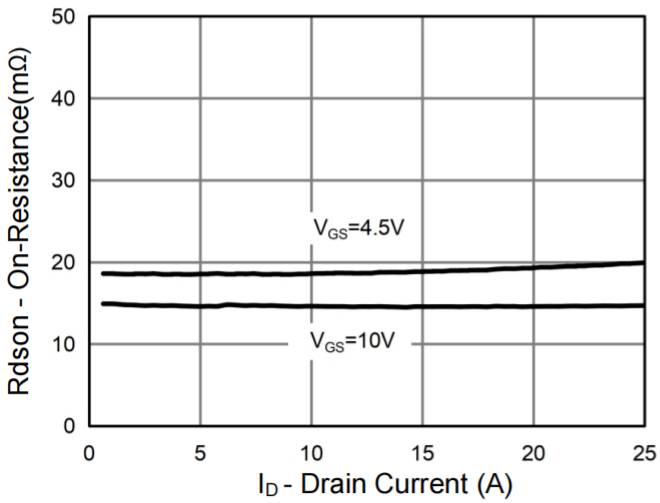


Figure 3 Rdson vs Drain Current

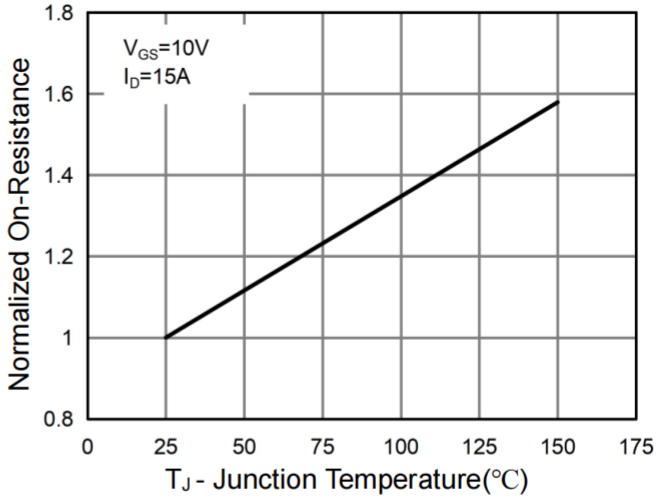


Figure 4 Rdson vs Junction Temperature

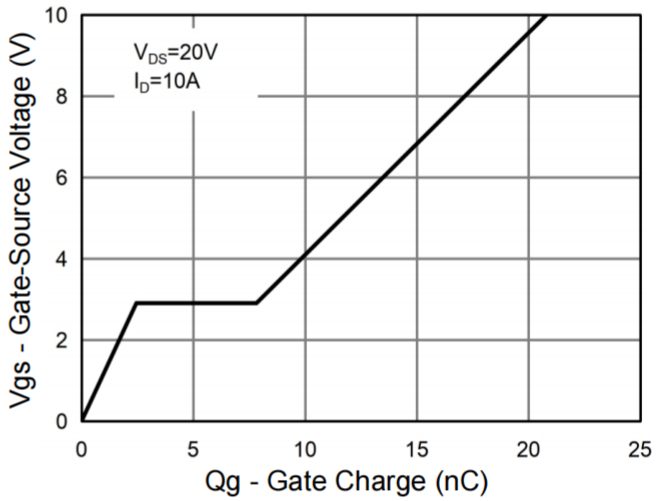


Figure 5 Gate Charge

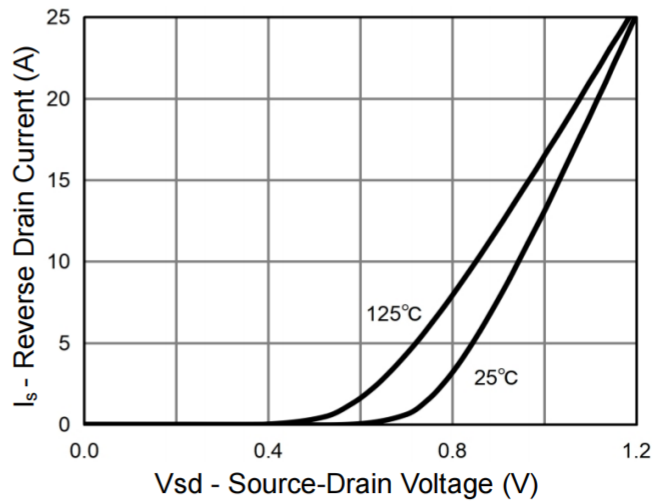


Figure 6 Source-Drain Diode Forward

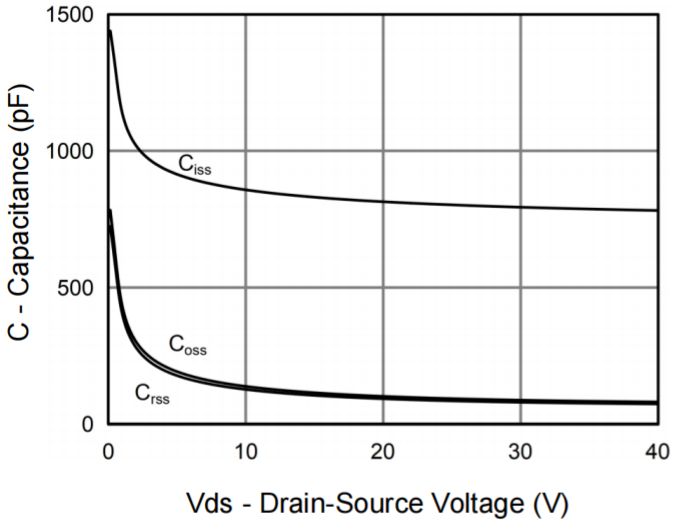


Figure 7 Capacitance vs Vds

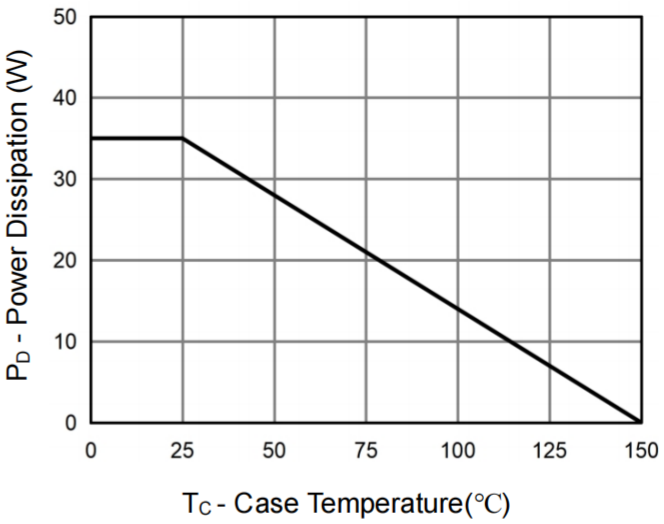


Figure 9 Power De-rating

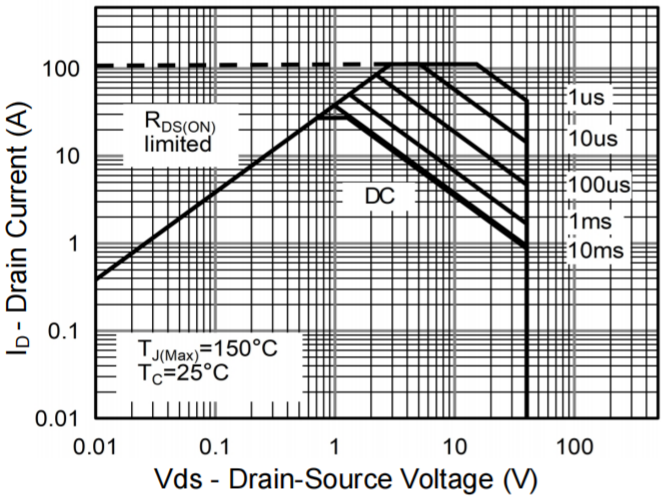


Figure 8 Safe Operation Area (Note 4)

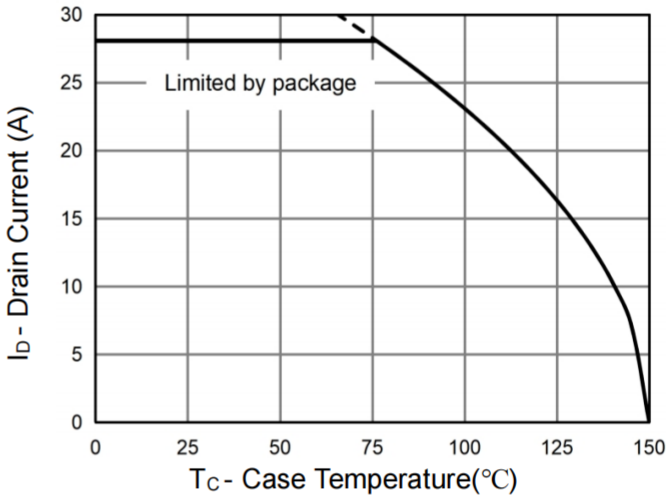


Figure 10 Drain Current De-ratin

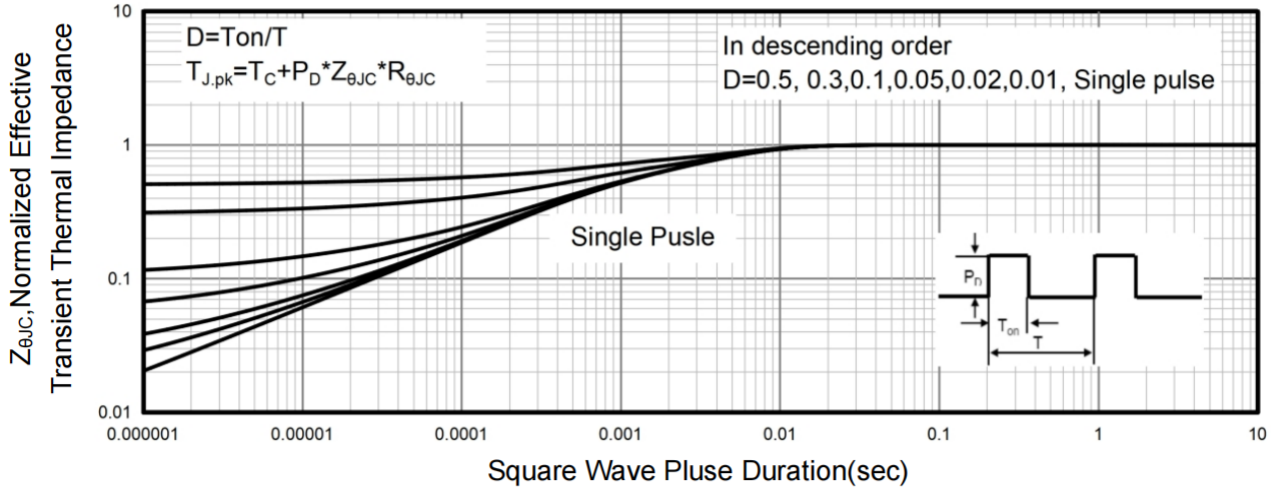
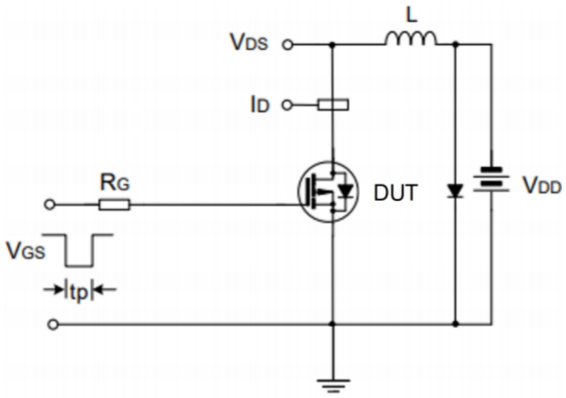


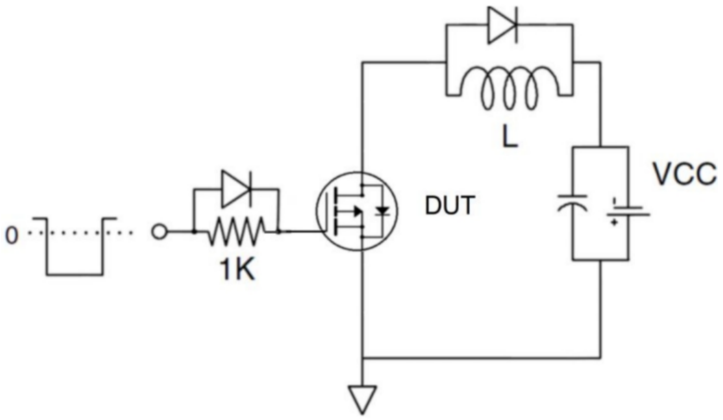
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

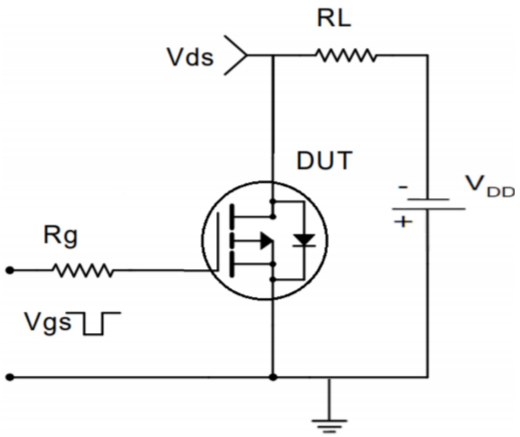
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



P-Channel Typical Electrical and Thermal Characteristics (Curves)

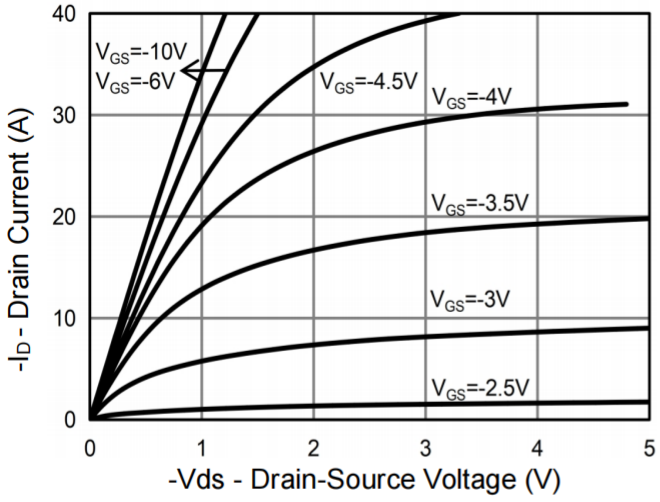


Figure 1 Output Characteristics

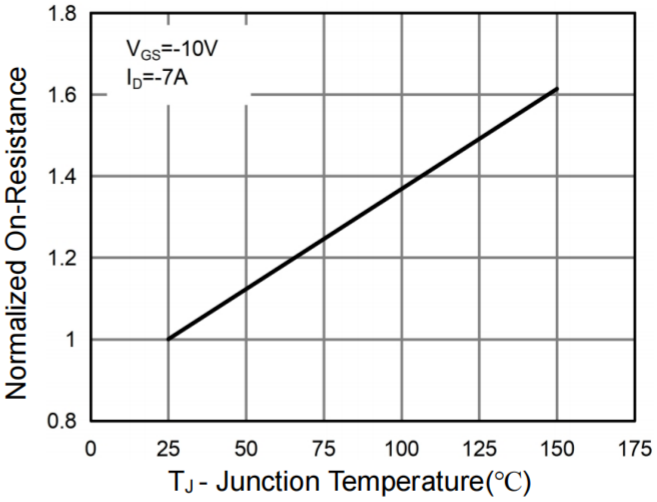


Figure 4 Rdson vs Junction Temperature

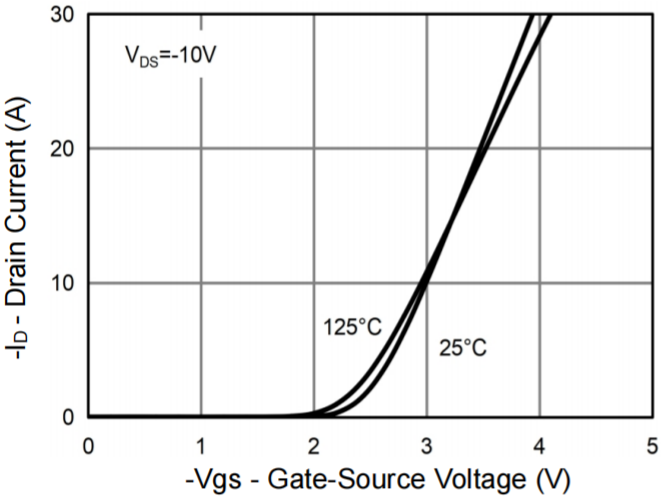


Figure 2 Transfer Characteristics

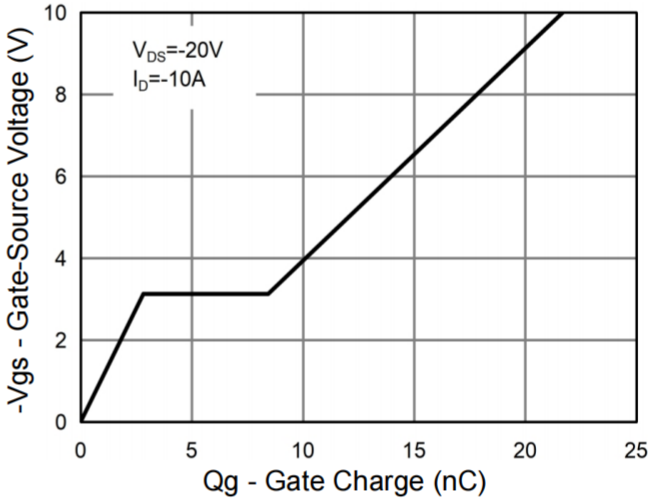


Figure 5 Gate Charge

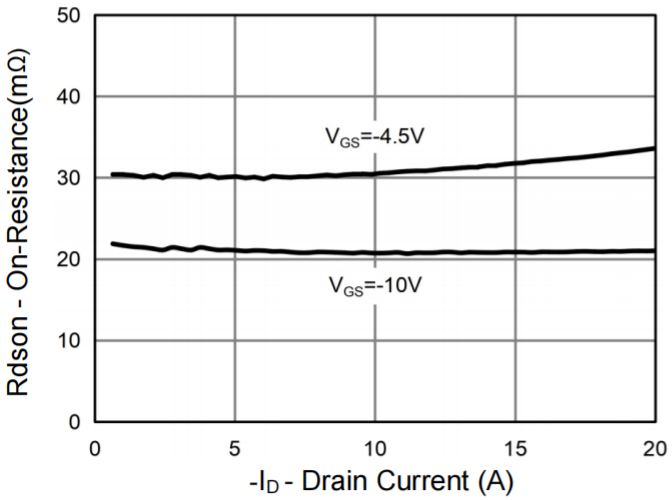


Figure 3 Rdson vs Drain Current

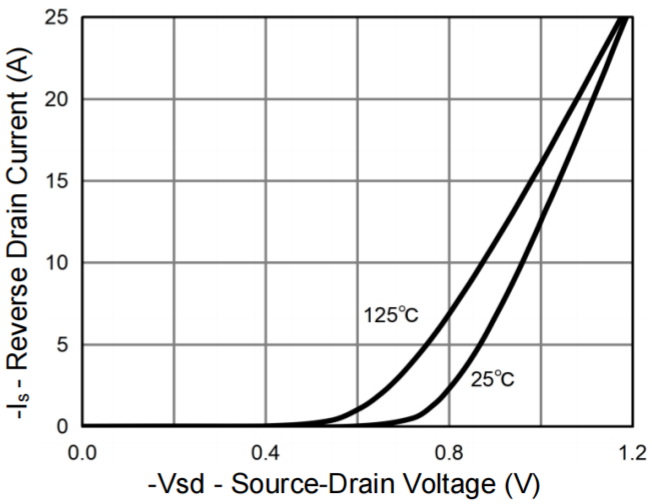


Figure 6 Source-Drain Diode Forward

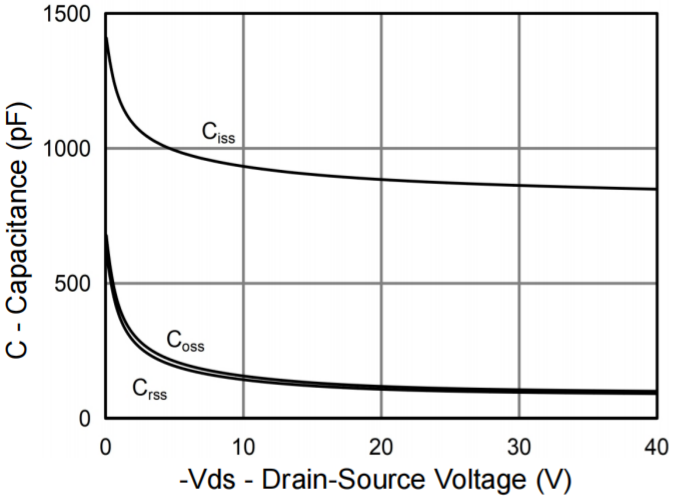


Figure 7 Capacitance vs Vds

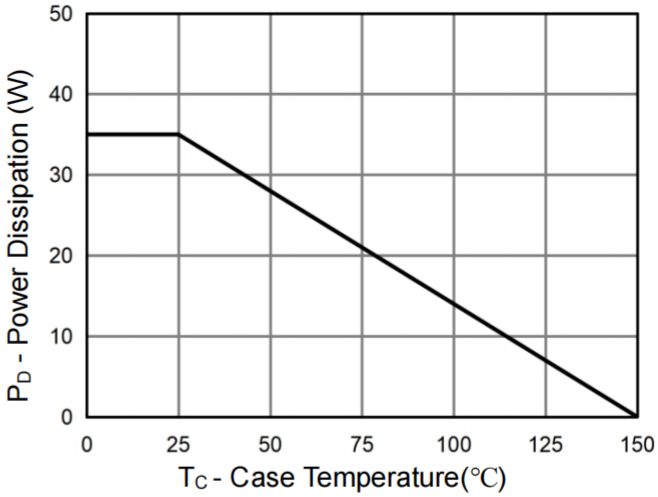


Figure 9 Power De-rating

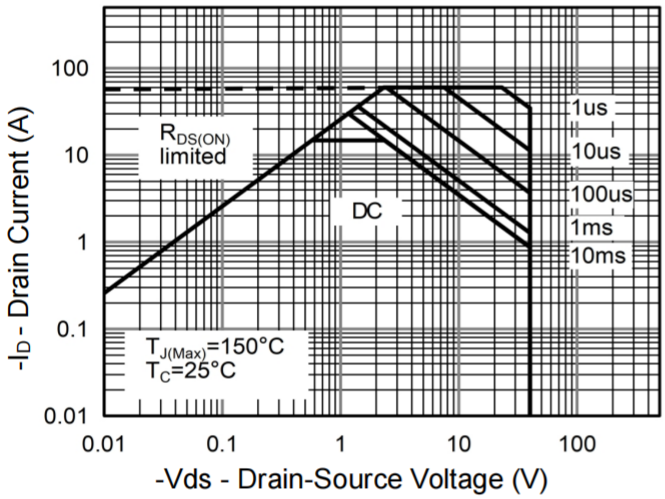


Figure 8 Safe Operation Area (Note 4)

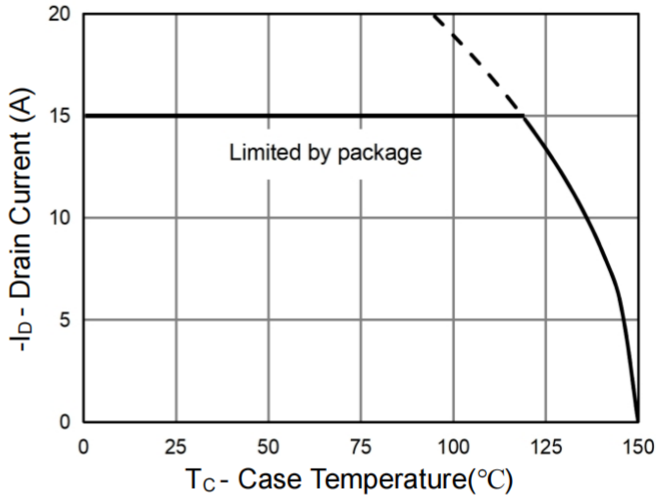


Figure 10 Drain Current De-rating

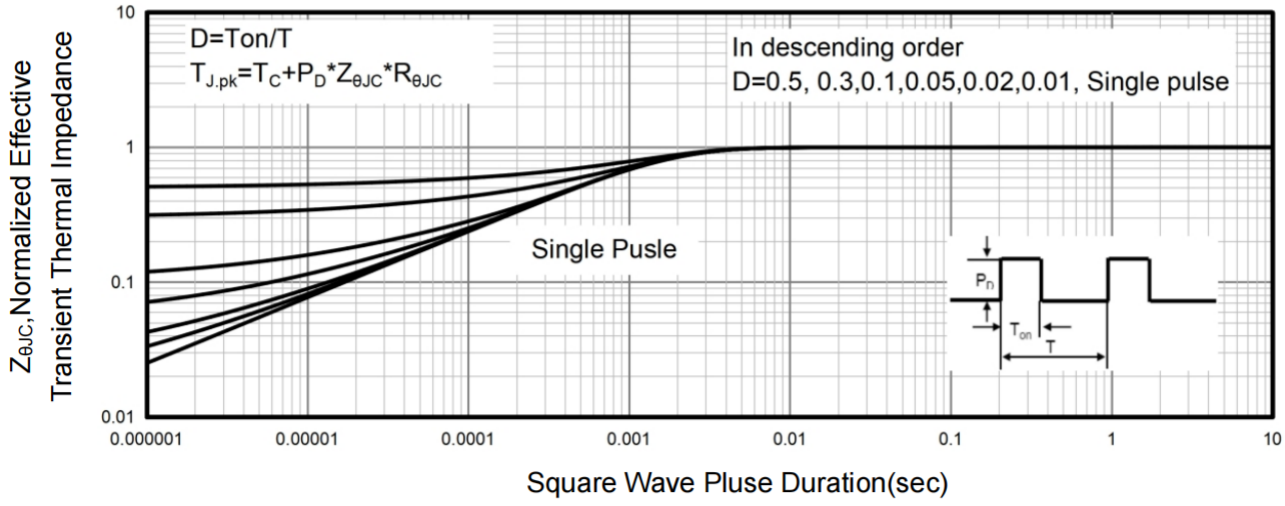
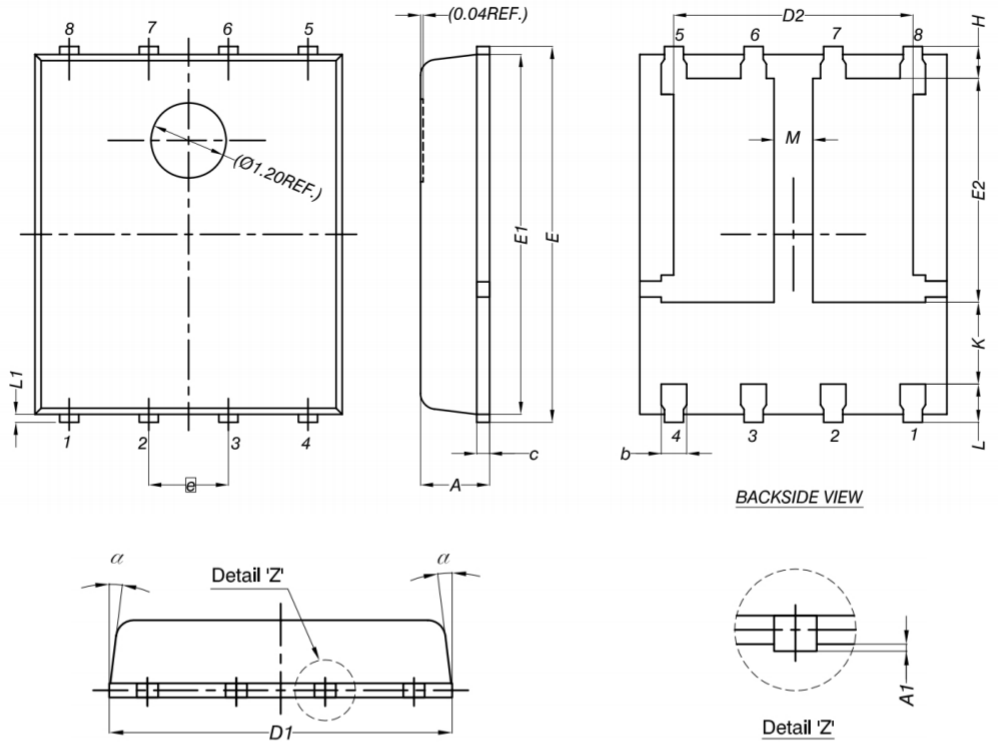
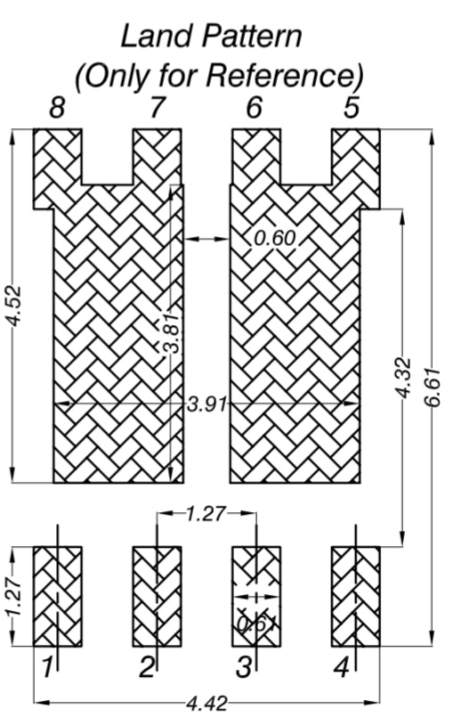


Figure 11 Normalized Maximum Transient Thermal Impedance

PDFN5×6-8L(G) Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	---	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.
   Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic
   Body Exclusive Of Mold Flash, Tie Bar , Tie Bar Burrs, Gate Burrs And Interlead Flash,
   But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.

Revision History

Revision	Date	Subjects
V4.0	2026.4	Update the parameters and curves.

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