

N and P-Channel Enhancement Mode Power MOSFET

Description

The NCE30NP07S uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

● N-Channel

$$V_{DS} = 30V, I_D = 6.5A$$

$$R_{DS(ON)} < 24m\Omega @ V_{GS}=10V$$

$$R_{DS(ON)} < 37m\Omega @ V_{GS}=4.5V$$

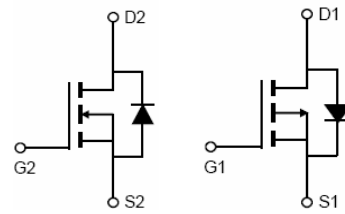
● P-Channel

$$V_{DS} = -30V, I_D = -7A$$

$$R_{DS(ON)} < 32m\Omega @ V_{GS}=-10V$$

$$R_{DS(ON)} < 70m\Omega @ V_{GS}=-4.5V$$

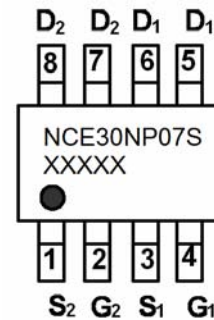
- High power and current handling capability
- Lead free product is acquired
- Surface mount package



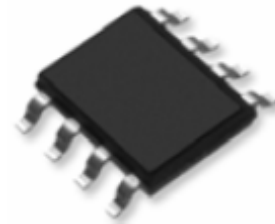
N-channel

P-channel

Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE30NP07S	NCE30NP07S	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V_{DS}	30	-30	V	
Gate-Source Voltage	V_{GS}	± 20	± 20	V	
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	6.5	-7	A
		$T_A=70^\circ\text{C}$	5.4	-5.8	
Pulsed Drain Current ^(Note 1)	I_{DM}	30	-30	A	
Maximum Power Dissipation	P_D	2.0	2.0	W	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	-55 To 150	$^\circ\text{C}$	

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note2)	$R_{\theta JA}$	N-Ch	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient ^(Note2)	$R_{\theta JA}$	P-Ch	62.5	$^\circ\text{C/W}$

N-CH Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30	33	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.6	3	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =6A	-	19	24	mΩ
		V _{GS} =4.5V, I _D =6A	-	26	37	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =6A	15	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	485.8	-	PF
Output Capacitance	C _{oss}		-	65.2	-	PF
Reverse Transfer Capacitance	C _{rss}		-	54	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, R _L =2.5Ω V _{GS} =10V, R _{GEN} =3Ω	-	4.0	-	nS
Turn-on Rise Time	t _r		-	2.0	-	nS
Turn-Off Delay Time	t _{d(off)}		-	14.0	-	nS
Turn-Off Fall Time	t _f		-	3.0	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =6A, V _{GS} =10V	-	12.6	-	nC
Gate-Source Charge	Q _{gs}		-	1.9	-	nC
Gate-Drain Charge	Q _{gd}		-	2.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =6A	-	0.8	1.2	V

P-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.3	-1.65	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-6.5A$	-	28	32	m Ω
		$V_{GS}=-4.5V, I_D=-6.5A$	-	49	70	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-6.5A$	10	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{ISS}	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	691.9	-	PF
Output Capacitance	C_{OSS}		-	113.7	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	109.4	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=2.3\Omega$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	7.5	-	nS
Turn-on Rise Time	t_r		-	5.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	19	-	nS
Turn-Off Fall Time	t_f		-	7	-	nS
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-6.5A$ $V_{GS}=-10V$	-	16.3	-	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	nC
Gate-Drain Charge	Q_{gd}		-	4.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-6.5A$	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

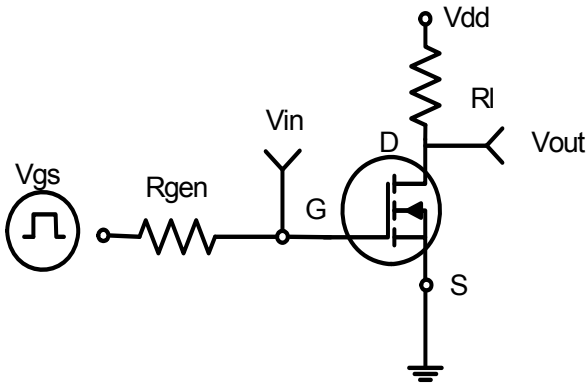


Figure 1: Switching Test Circuit

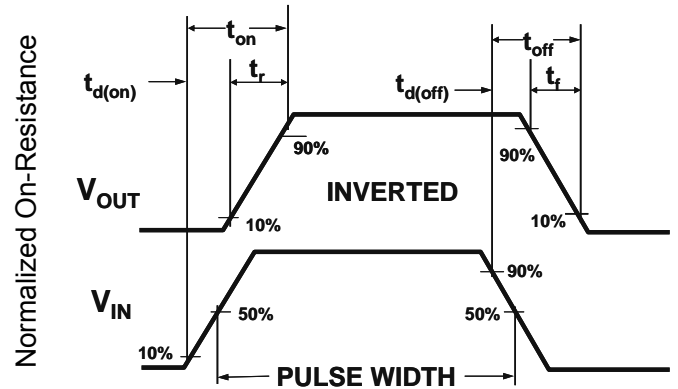


Figure 2: Switching Waveforms

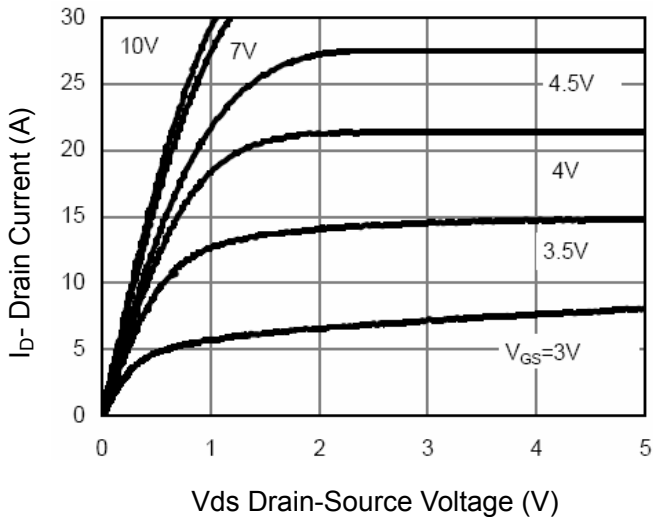


Figure 3 Output Characteristics

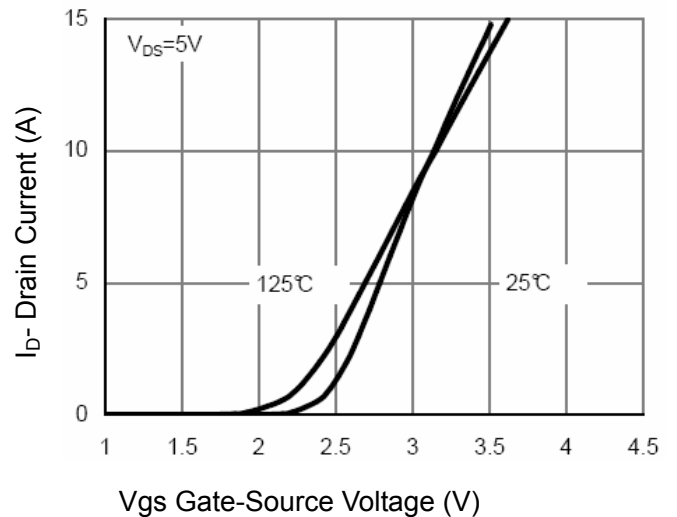


Figure 4 Transfer Characteristics

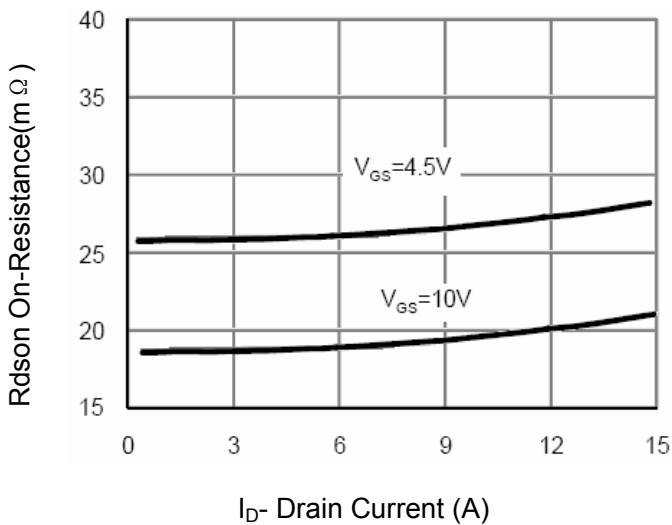


Figure 5 Drain-Source On-Resistance

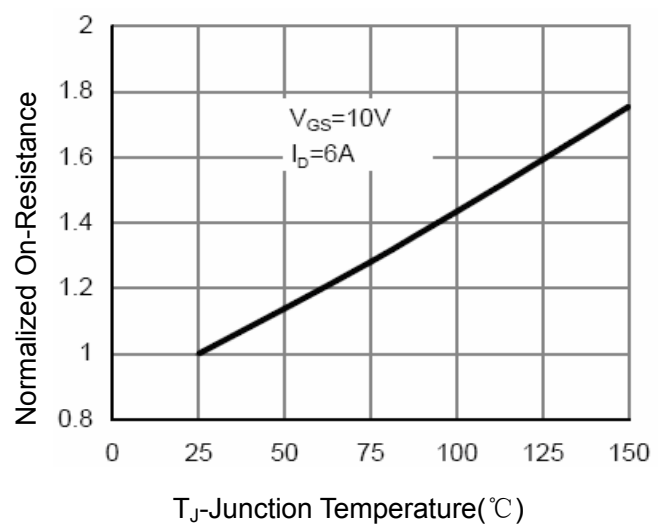
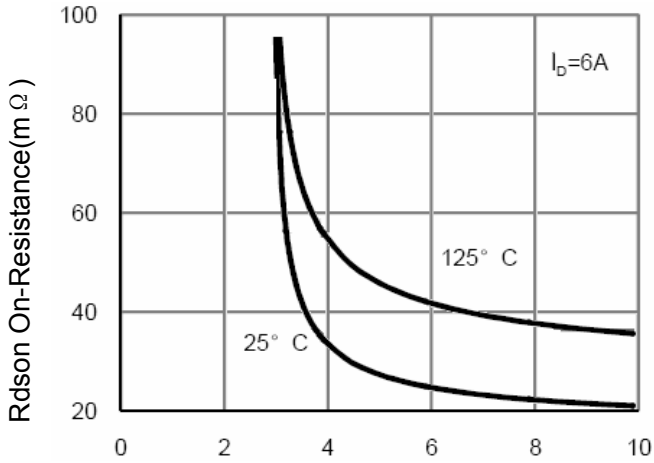
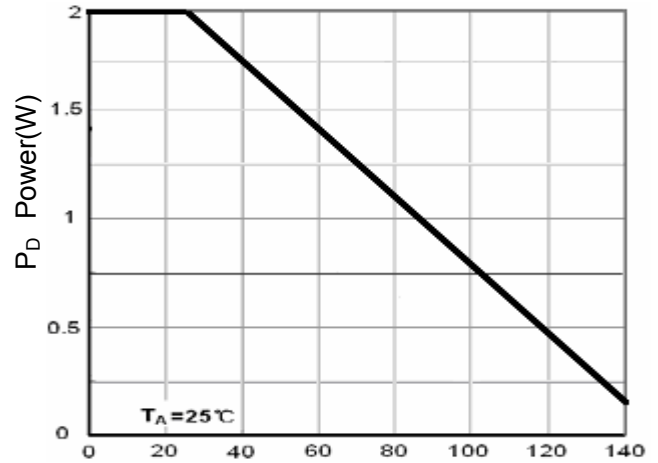


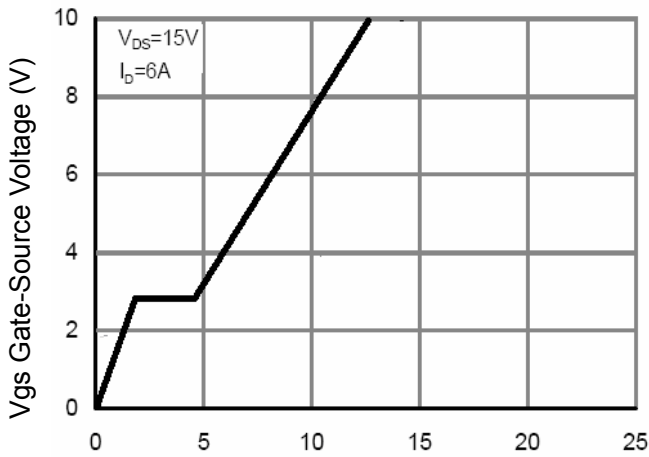
Figure 6 Drain-Source On-Resistance



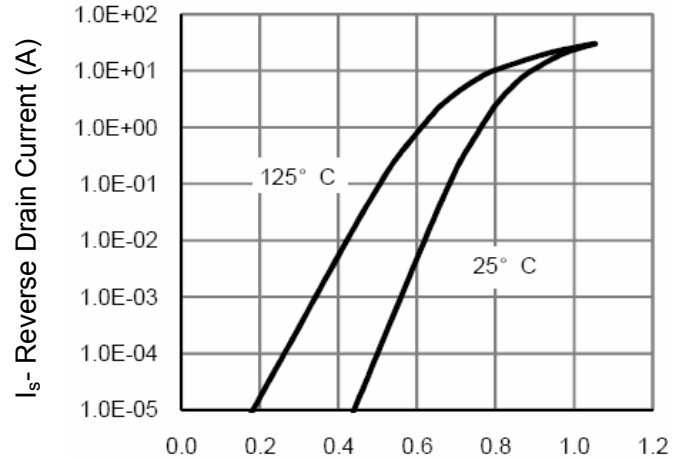
Vgs Gate-Source Voltage (V)
Figure 7 Rdson vs Vgs



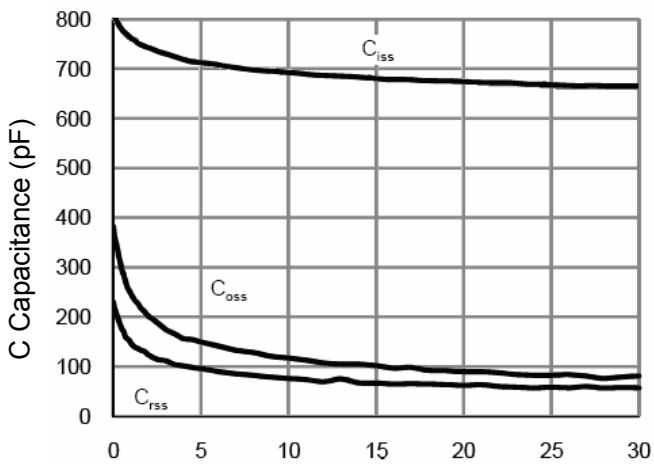
Tj Junction Temperature (°C)
Figure 8 Power Dissipation



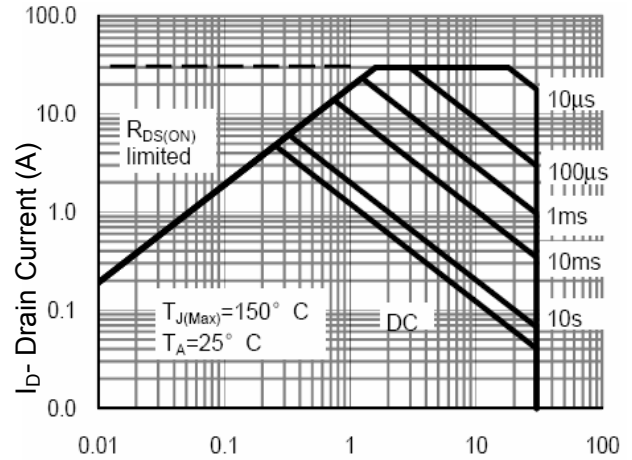
Qg Gate Charge (nC)
Figure 9 Gate Charge



Vds Drain-Source Voltage (V)
Figure 10 Source- Drain Diode Forward



Vds Drain-Source Voltage (V)
Figure 11 Capacitance vs Vds



Vds Drain-Source Voltage (V)
Figure 12 Safe Operation Area

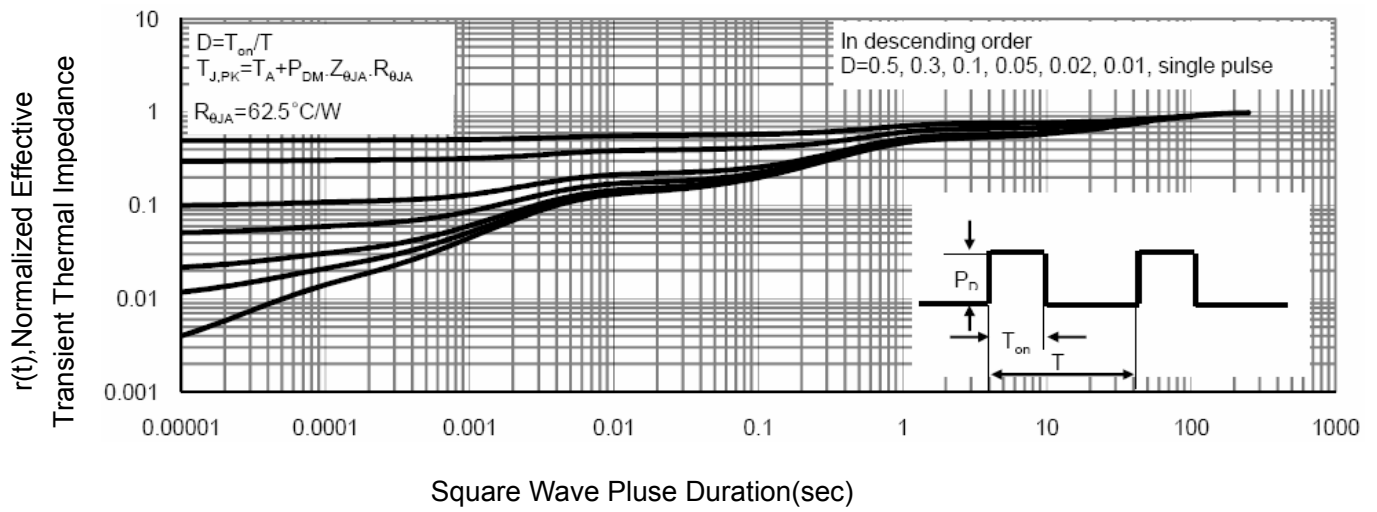


Figure 13 Normalized Maximum Transient Thermal Impedance

P- Channel Typical Electrical and Thermal Characteristics (Curves)

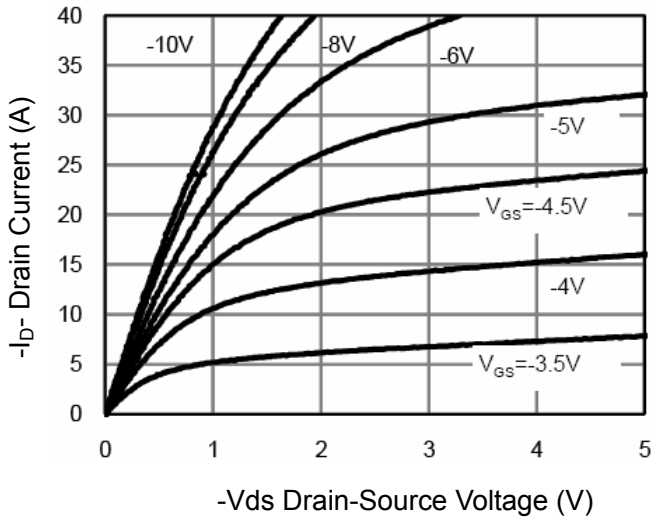


Figure 1 Output Characteristics

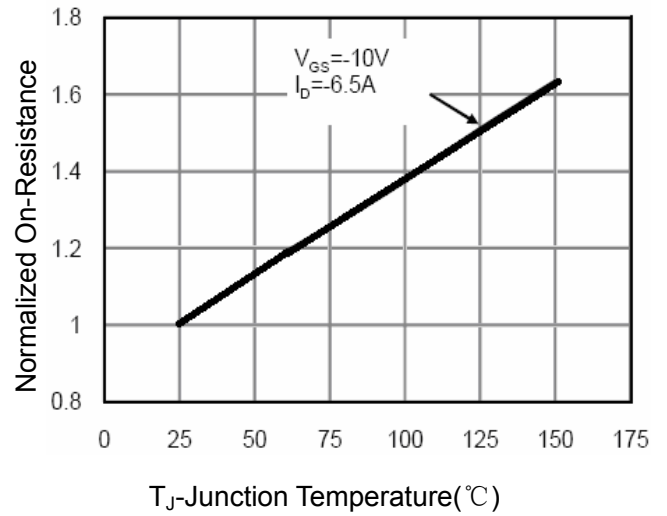


Figure 4 Rdson-Junction Temperature

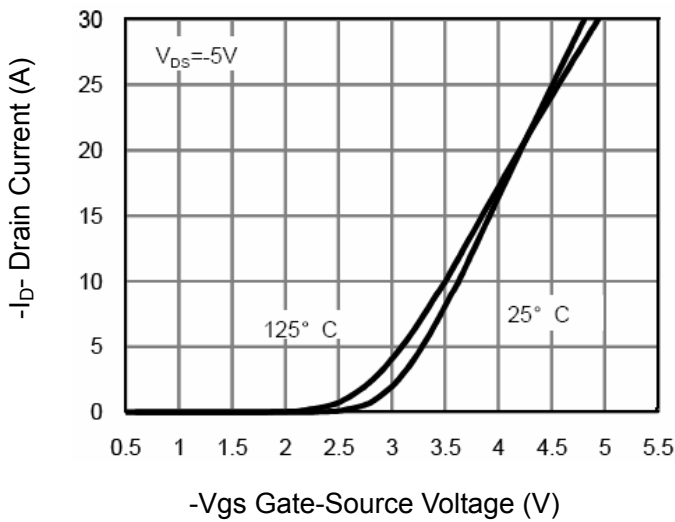


Figure 2 Transfer Characteristics

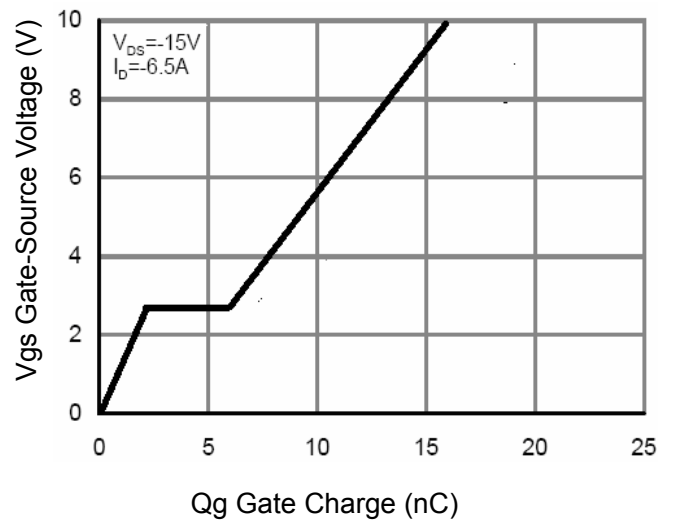


Figure 5 Gate Charge

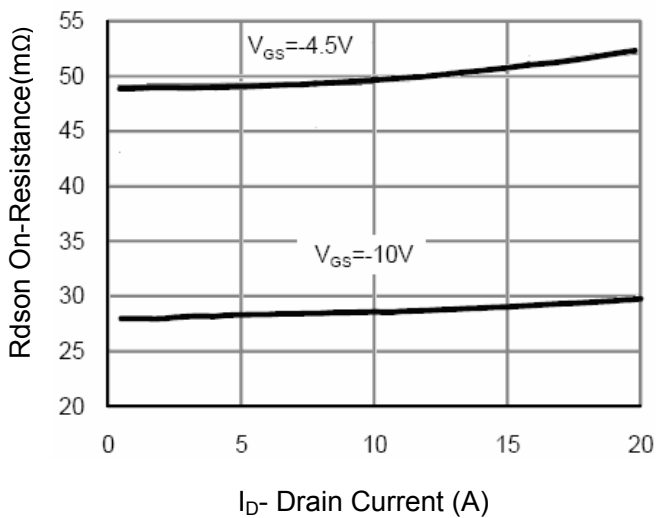


Figure 3 Rdson- Drain Current

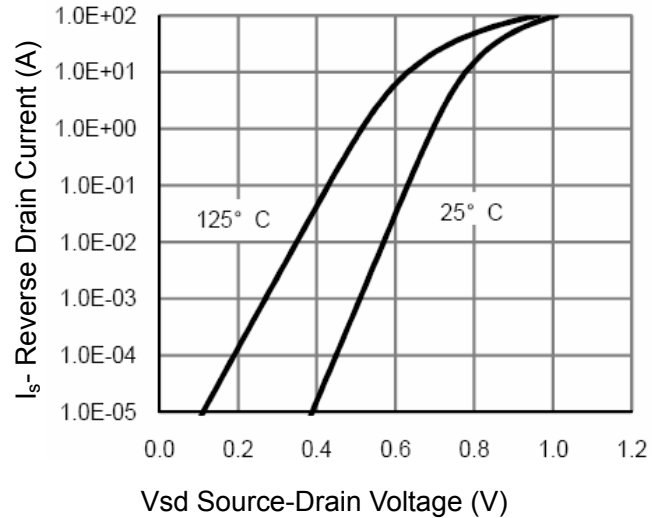


Figure 6 Source- Drain Diode Forward

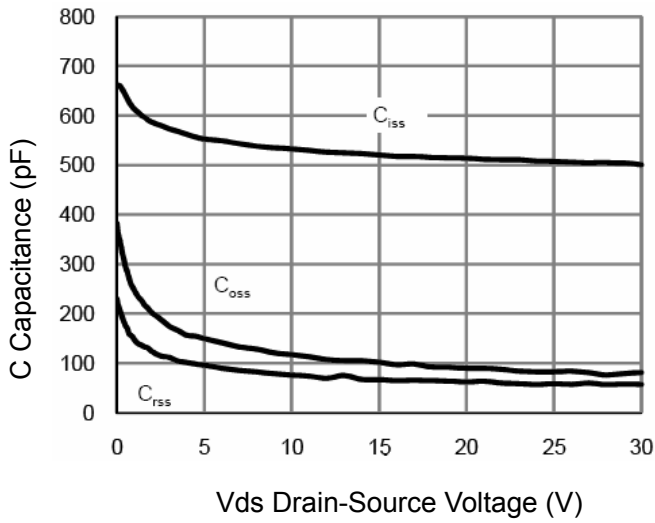


Figure 7 Capacitance vs Vds

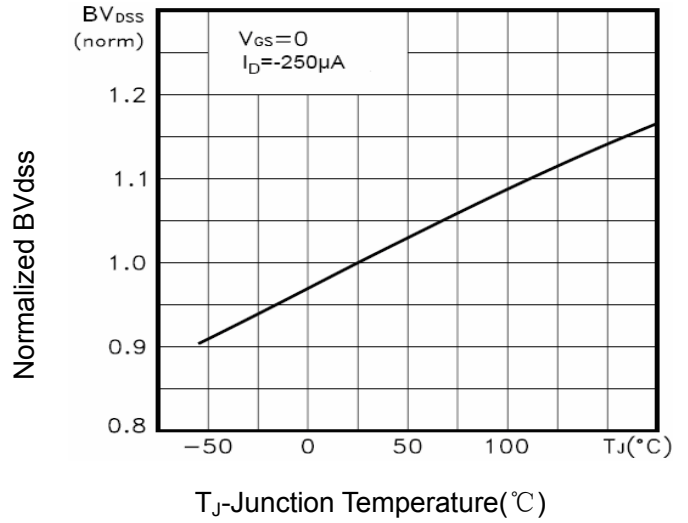


Figure 9 BV_{DSS} vs Junction Temperature

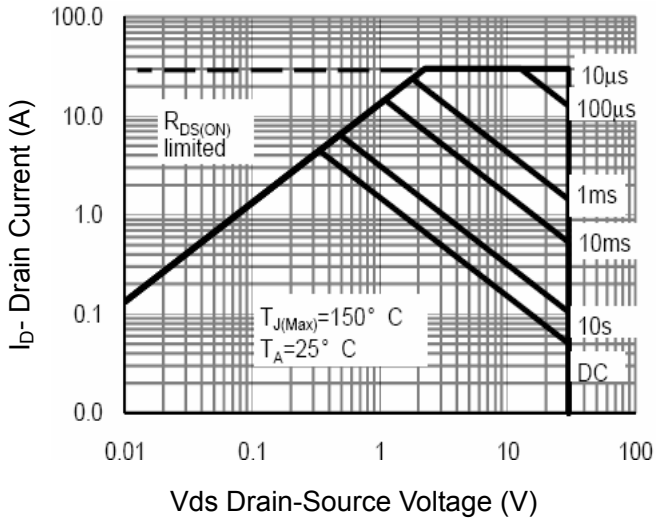


Figure 8 Safe Operation Area

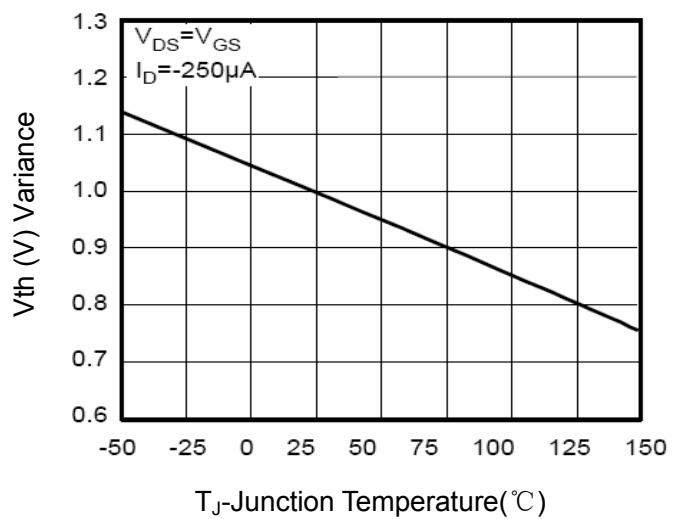


Figure 10 V_{GS(th)} vs Junction Temperature

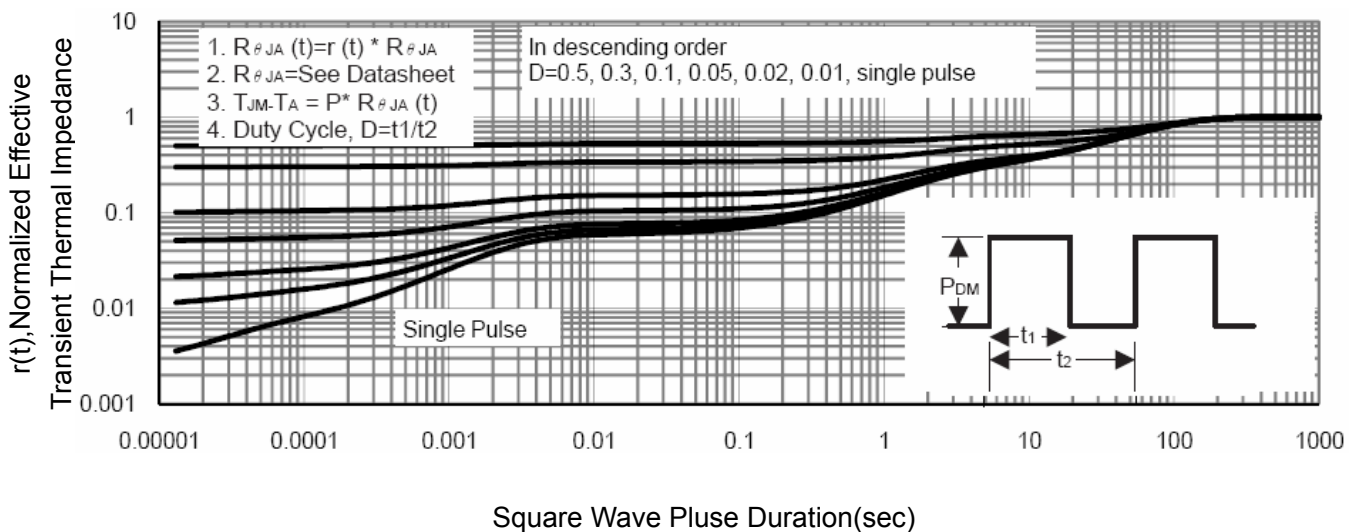
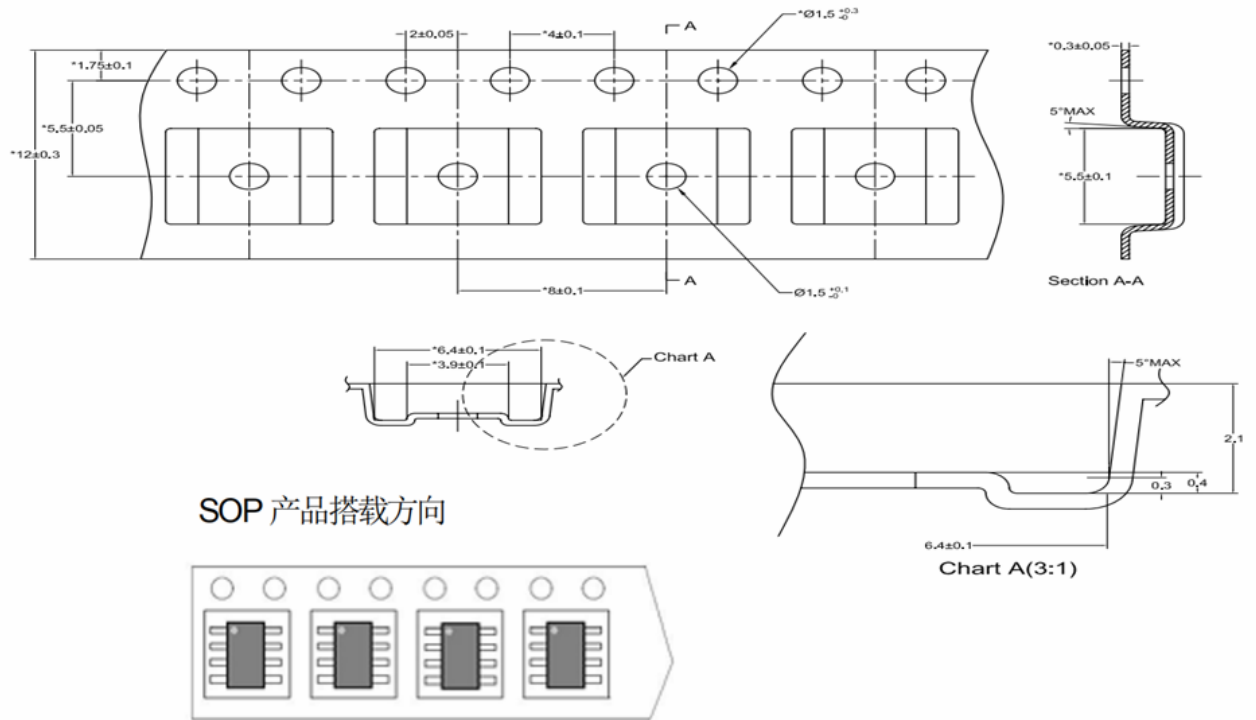


Figure 11 Normalized Maximum Transient Thermal Impedance

一、载带图纸与产品搭载方向示意图：



二、包装信息表（满箱信息）

封装形式	包装方式	盘尺寸	只/盘	盘/内盒	只/内盒	内盒/箱	只/箱
SOP8	编带	13寸	4000	1	4000	5	20000

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